

In the specification

Please replace the paragraph beginning on page 5, line 9 of the specification with the paragraph below. The paragraph is amended to correct an error identifying transistor 47 as a PMOS transistor. As noted elsewhere in the originally-filed application, transistor 47 is an n-type MOS transistor. See Application, p. 7, ln. 15-16, claim 2, and Figs. 1 and 2. Added text is underlined, deleted text has been struck through.

The external voltage available at terminal 25 is the same voltage available at terminal 11 and is also available to the ~~native-PMOS~~ NMOS transistor 47 along 49. The internal reference voltage along 35 is transferred to line 45 connected to the gate of transistor 47 which preferably has a conduction threshold of approximately zero volts. the output of transistor 47 is taken along line 51 and is another internal reference voltage feeding the high current and noisy low voltage circuits 53. Transistor 47 feeds a load 53 directly and can be scaled to handle sufficient current for the load. Alternatively, parallel transistors, constructed identically to transistor 47 can feed similar loads at other locations on an integrated circuit chip.